**Name**: Samya Sunibir Das

**ID**: 1911563642

**Course and Section**: CSE332.3

**Submission Date**: 14th January 2020

**Lab 8 Discussion**

1. Lab 8 Discussion – Datapath Design

In the eighth lab class, we were demonstrated the full-fledged design of a single cycle datapath. The datapath is an important part of a processor, since it implements the fetch-decode-execute

cycle. In order to implement the design, we used the 16 bit ALU that we designed in the earlier class and also the 16 bit register that we also had finished weeks ago. We used RAM (volatile memory) and ROM (non-volatile memory) in this design. ROM conducted only read operations whereas the RAM conducted read and write both. The ROM here is used to pass instruction and connected to the program counter, PC. PC stores the address of the current instruction. 16 bit output is generated whenever PC value is incremented by 1. It subsequently moves on to the decoding part then. The datapath we have designed can handle R, I type instructions. The ALU came in to play when it was time to execute. The result of ALU was connected to the RAM to store the result. When it comes to Write Back, we will pass the instruction or the ALU result to write in register based on what instruction type with the help of the MUX we used here. The class concluded by instructing us to submit the discussion in google classroom and the circuit files for the datapath design in git.